J. KELLY FLANAGAN

Dean, Smith College of Engineering and Technology
Utah Valley University
Orem, Utah 84058

Email: kelly@flanagan.io
Phone: 801-369-0033

I am an experienced educator, researcher, and academic administrator. As a professor of computer science, I created several innovative courses, won the teacher of the year award, won a highly competitive National Science Foundation grant, published numerous technical papers, mentored undergraduate students, advised graduate students, and served in administrative positions. As a university vice president and chief information officer, I led thousands of people, created and managed $100 million budgets, wrote successful funding proposals, led the design, funding, and construction of two university buildings, and created physical and organizational environments where academic and administrative innovation flourishes. As a college dean, I created a culture of truth, trust, and transparency; recruited, hired, retained, and promoted faculty; and raised over $30 million in gifts.

EDUCATION

Ph.D., August 1993, Brigham Young University, Electrical and Computer Engineering
Dissertation: A New Methodology for Accurate Trace Collection and Its Application to Memory Hierarchy Performance Modeling

M.S., August 1989, Brigham Young University, Electrical Engineering
Thesis: Processor Design Using Path Programmable Logic

B.S., April 1988, Brigham Young University, Electrical Engineering

ADMINISTRATIVE EXPERIENCE

Dean, Smith College of Engineering and Technology, Utah Valley University, June 2022–Present

- Responsible for the leadership and management of the academic and administrative functions of the college and its 11 academic departments, nearly 100 academic programs, and 6800 majors.
- Responsible for developing college strategic initiatives and providing senior-level administrative leadership in curriculum development, institutional assessment and improvement, human resource, faculty development and performance appraisals, budget and finance, and facilities planning and management
    - Increased college majors by 11% in the last two years
    - Proposed and gained support for a common college-wide retention, tenure, and promotion (RTP) criteria document
    - Introduced undergraduate and graduate programs in Cybersecurity and Applied Artificial intelligence (AI)
    - Divided, merged, and reorganized multiple departments to enhance student engagement, retention, and completion
- Responsible for developing, proposing, and acquiring college budgets of $40 million
- Responsible for fundraising and cultivating relationships with industry partners and donors
    - Responsible for the funding, design, and construction of a 184,000 sq ft engineering and technology building
    - Participated in the naming of our new building and raising the associated $25 million gift
- Leader in university long-term planning and policy setting
- Report to the Provost
- Member of the Academic Affairs Council

Vice President of Digital Transformation and CIO, Utah Valley University, 2020–2022

- Responsible for the digital transformation of UVU processes, culture, and technology
- Responsible for the vision, strategy, policy, guidelines, planning, coordination, and oversight of academic and administrative information technology for UVU
- Responsible for the appropriation, revenue, and expenditures of a $20 million budget
- Work closely with other Vice Presidents, Deans, Faculty Senate, and other faculty and staff to help them effectively use IT to achieve their purposes and advance their strategies
- Participate in the creation and development of university policy, procedures, planning, and the development of the annual university budget request
- Direct the activities of the Office of Information Technology and Academic and Student Digital Services
- Report to the president
- Member of the President's Cabinet and various subcommittees

Chief Information Officer (CIO), Church Educational System (CES) of the Church of Jesus Christ of Latter-day Saints, 2015–2020

- Responsible for the vision, strategy, policy, guidelines, planning, coordination, and oversight of information technology (IT) for the CES institutions of higher education (3,800 faculty and 84,000 students at five institutions)
- Responsible for the system-wide CIO budget of $100 million
- Report to the Commissioner of Education
- Work with the presidents, vice presidents, and CIOs of the CES institutions to develop solutions to resolve institutional issues
- Chair the CES CIO Committee consisting of the CIOs from each CES institution
- Approve institutional IT budgets for inclusion in the CES budget request presented to the Board of Trustees
- Specific accomplishments include:
    - Proposed a strategy and implementation plan to use artificial intelligence systems to identify and rescue academically at-risk students at BYU-Idaho
    - Established a CES Networking Center that provides high-quality network services for BYU, BYU-Hawaii, and BYU-Idaho
    - Acquired and modified an open-source eTextbook reader to enhance the quality of instruction and reduce the cost of education
    - Worked with faculty leadership at each institution to adopt a standard learning management system that reduces overall cost and makes sharing content easier
    - Created an IT security strategy, architecture, and implementation that provides consistent, high-quality security for each institution
    - Established and refined a model for funding IT projects, the acquisition of commercial software, and ongoing maintenance of IT infrastructure
    - Developed an ecclesiastical endorsement system to allow the institutions to receive student status information from religious leaders in a private, appropriate, and legal manner
    - Implemented a CES Shared Application that enables applicants to apply to one or more of the institutions through a single application

Vice President, Information Technology and CIO, Brigham Young University, 2002–2020

- Responsible for the vision, strategy, policy, guidelines, planning, coordination, and oversight of academic and administrative information technology for BYU (1,630 faculty and 34,240 students)
- Responsible for CIO budget of $70 million
- Report to the president

- Member of the President's Council and various subcommittees such as the Human Resource Committee and the Campus Planning and Use Committee
- Work closely with other Vice Presidents, Deans, Faculty Advisory Council, and other faculty and staff to help them effectively use IT to achieve their purposes and advance their strategies
- Participate in the creation and development of university policy, procedures, planning, and the development of the annual university budget request
- Direct the activities of the Office of Information Technology, the Print and Mail Production Center, and the Office of Research Computing (300 full-time and 1000 student employees)
- Specific accomplishments include:
    - Initiated a Domain of One's Own initiative that has taught over 6,000 students basic Internet technology, how to select a professional Internet domain name and use it to publish content of their own
    - Developed a vision statement describing how to implement online education in a way that improves the quality of instruction, reduces cost, reduces time to graduation, and allows more students to be taught with the same resources
    - Led an effort to replace expensive proprietary hardware in over 700 technology-enabled classrooms with open-source commodity components, saving $400,000 annually
    - Defined a University Application Programming Interface (API) that enables faculty, staff, students, and organizations to easily interact with university information, data, and processes without violating university policy or procedures
    - Created a culture and practice of IT excellence that enticed others to participate in centralized services rather than mandating compliance
    - Received a commendation in BYU's accreditation reaffirmation from the Northwest Commission on Colleges and Universities "for the effective use of information technology"
    - Proposed and oversaw the construction of a 40,000 sq ft building to house the Office of Information Technology, a 12,000 sq ft data center to house computing infrastructure for BYU and the Church of Jesus Christ of Latter-day Saints, and a high-performance computing data center to house the Ira A. Fulton Supercomputing Laboratory
    - Developed the strategy that led to the selection and acquisition of technology that enabled BYU Broadcasting to become a premier award-winning university broadcasting organization
    - Led a team of individuals from Athletics, Special Events, and IT to acquire approval and funding for the BYU Marriott Center scoreboard, WiFi in the Marriott Center, and WiFi in LaVell Edwards Stadium
    - Developed the Administrative Mission, Vision, and Values document used at BYU

Associate Chair, Department of Computer Science, Brigham Young University, 2000–2002
- Assisted and advised the Chair on all matters of substance
- Assisted in the faculty hiring process
- Participated in Department budget preparation

Graduate Coordinator, Department of Computer Science, Brigham Young University, 1999–2000
- Assisted and advised the Chair on matters related to graduate education and research
- Represented the Department in meetings with Graduate Studies and the Associate Academic Vice President for Research
- Validated the completion of each graduate student's coursework and thesis or dissertation
- Enhanced and maintained the Department's Graduate Handbook

ACADEMIC EXPERIENCE

Dean, Smith College of Engineering and Technology, Utah Valley University, June 2022-Present
Professor, Computer Science, Utah Valley University**,** 2020–present

Emeritus Professor, Computer Science, Brigham Young University**,** 2020–present
Professor, Computer Science, Brigham Young University**,** 2004–2020
Associate Professor, Computer Science, Brigham Young University, 1999–2004
Assistant Professor, Computer Science, Brigham Young University, 1993–1999
Visiting Professor and Researcher, High-Performance Computer Architecture Group, Intel Corporation, Hillsboro, Oregon, 1993–1994
Instructor, High Performance Computer Architecture, Oregon State University, Corvallis, Oregon, 1994

SERVICE

EXTERNAL

Member, Trustland Committee, Karl G. Maeser Preparatory Academy, 2020-2024
Founder and Chair, Internet of Things (IoT) Workshop, 2016–2020
Founder and Chair, University API (UAPI) Workshop, 2015–2020
Member, Academic Review Board for Computer and Information Sciences Department of Brigham Young University–Hawaii, 2015
Member, Academic Review Board for Computer and Information Sciences Department of Brigham Young University–Hawaii, 2011
Member, Utah Innovation Awards Devices Committee, 2016
Chair, Utah Innovation Awards Devices Committee, 2015
Reviewer, Numerous IEEE and ACM journals and conference proceedings
Reviewer, Numerous National Science Foundation grant proposals

CHURCH EDUCATIONAL SYSTEM

Member, CES Presidents' Roundtable, 2015–2020
Chair, CES CIO Committee, 2015–2020
Member, CES Budget Review Committee, 2015–2020
Member, Institutional Budget Review Committee, 2015–2020

UNIVERSITY

Member, UVU Strategic Relations Council, 2023-present
Member, UVU Academic Affairs Council, 2022-present
Member, UVU Deans Committee, 2022-present
Member, UVU President's Cabinet, 2020-2022
Member, UVU President's Council, 2020-2022
Member, BYU President's Council, 2002–2020
Chair, BYU Information Technology Policy Committee (ITPC), 2002–2020
Member, BYU Online Committee, 2016–2020
Member, BYU Academic Vice President Search Committee, 2017
Member, BYU Academic Vice President Search Committee, 2010
Chair, BYU Information Technology Resources Committee (ITRC), 2000–2002

COLLEGE

Chair, BYU College of Physical and Mathematical Sciences Computing Committee, 2000–2002

DEPARTMENT

Member, BYU Computer Science Faculty Search Committee, 2000–2002

Chair, BYU Computer Science Department Computing Committee, 1996–1999
Member, BYU Computer Science Department Computing Committee, 1993–1996

COURSES TAUGHT

Embedded Systems and Set Top Boxes, CS 598R, Brigham Young University, 2003
Advanced Computer Architecture, CS 580, Brigham Young University, 1995–2002
Advanced Computer Architecture, ECE 570, Oregon State University, 1994
Computer Architecture, CS 380, Brigham Young University, 1994–2000
Computer Organization, CS 143, Brigham Young University, 1998–2000
Book of Mormon, Rel 121, Brigham Young University, 2004

PROFESSIONAL AFFILIATIONS

Association for Computing Machinery (ACM)
Institute of Electrical and Electronics Engineers (IEEE)
Special Interest Group on Computer Architecture (SIGARCH), ACM
Special Interest Group on Measurement and Evaluation (SIGMETRICS), ACM
EDUCAUSE

AWARDS AND HONORS

Honored Alumnus, Electrical and Computer Engineering, BYU, 2012
Distinguished Contributions to Accessibility, BYU, 2005
Golden Key Award, Utah Citizen of the Year, 2000
Teacher of the Year, Department of Computer Science, BYU, 1998
Honored Student Award, College of Engineering, BYU, 1988

PATENTS

Flanagan et al. 2016. Systems and methods for secure intermediary data transfers using close proximity wireless communication. U.S. Patent 9,397,728, filed June 15, 2015, and granted July 19, 2016

Flanagan et al. 2015. Systems and methods for establishing secure communication using close proximity wireless communication. U.S. Patent 9,088,864, filed October 3, 2013, and granted July 21, 2015

Flanagan et al. 2015. Systems and methods for secure intermediary data transfers using close proximity wireless communication. U.S. Patent 9,084,078, filed October 3, 2013, and granted July 14, 2015

RESEARCH FUNDING

A National Trace Collection and Distribution Resource, $1,529,978, National Science Foundation, 1998
IA-32 Trace Collection and Workload Characterization, $42,500, Hewlett-Packard, 1998
Performance Evaluation of Multiprocessor Architectures, $26,000, Hewlett-Packard,1998
Performance Surface Analysis of Wide Area Distributed Systems, $150,000, Sprint Corporation, 1997
Using ATM Networks for High Performance Computing, $100,000, Sprint Corporation, 1996
Analysis of I/O Activity in Novell NetWare Clients and Server, $30,000, Intel Corporation, 1996
Generating R4400 Instruction Traces, Tandem Corporation, $25,000, 1996
Analysis of Disk Activity in A Novell NetWare Environment, Intel Corporation, $30,000, 1995

PUBLICATIONS

JOURNALS

M. Clement, G. Judd, B. Morse, and K. Flanagan, Performance Surface Prediction for WAN-based Clusters, Journal of Supercomputing, Vol. 13, 1999.

K. Flanagan, J. Archibald, and J. Su, Low Power Memory Hierarchies: An Argument for Second-Level Caches, Microprocessors and Microsystems, Vol. 21, No. 5, February 1998.

K. Grimsrud, J. Archibald, M. Ripley, K. Flanagan, and B. Nelson, BACH: A Hardware Monitor for Tracing Microprocessor Based Systems, Microprocessors and Microsystems, Vol. 17, No. 8, October 1993.

T. Li, B. Nelson, and K. Flanagan, CMOS Implementation of a Correlator for Delta-Modulated Signals, International Journal of Electronics, Vol 67, No. 2, 1989.

CONFERENCE PROCEEDINGS

Myles G. Watson and Kelly Flanagan. "System-Level Prototyping with HyperTransport." In Proceedings of the Second International Workshop for HyperTransport Research and Applications 2011 (WHTRA2011), Mannheim, Germany, February 2011.

M. Watson and J. K. Flanagan. “Designing Large Memories with Hardware Prototyping.” Workshop on Architectural Research Prototyping, Held in conjunction with ISCA, July 2006.

Myles G. Watson and J. Kelly Flanagan, Does Halting Make Trace Collection Inaccurate? A Case Study Using Pentium 4 Performance Counters and SPEC2000, In Proceedings of the Seventh IEEE Annual Workshop on Workload Characterization, October 2004.

Elizabeth S. Sorenson and J. Kelly Flanagan, Evaluating Synthetic Trace Models Using Locality Surfaces, Fifth Annual IEEE Workshop on Workload Characterization (WWC-5), Austin Texas, November 2, 2002, pp 23–33.

Myles Watson and J. Kelly Flanagan. Simulating L3 Caches in Real Time Using Hardware Accelerated Cache Simulation (HACS): a Case Study with SPECint 2000, In Proc. 14th Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Vitoria, ES, Brazil, October 2002, pp. 108–114.

Elizabeth S. Sorenson and J. Kelly Flanagan, Cache Characterization Surfaces and Predicting Workload Miss Rates, Fourth Annual IEEE Workshop on Workload Characterization (WWC-4), Austin Texas, December 2, 2001.

Elizabeth S. Sorenson and J. Kelly Flanagan. Using Locality Surfaces to Characterize the SPECINT 2000 Benchmark Suite. In Lizy Kurian John and Ann Marie Grizzaffi Maynard, editors, *Workload Characterization of Emerging Computer Applications*, pages 101–120. Kluwer Academic Publishers, 2001.

Niki C. Thornock and J. Kelly Flanagan, Facilitating Level Three Cache Studies Using Set Sampling, Proceedings of the 2000 Winter Simulation Conference, Vol. 1, pp 471–479.

Niki C. Thornock and J. Kelly Flanagan, Using the BACH Trace Collection Mechanism to Characterize the SPEC 2000 Integer Benchmarks, Third Annual IEEE Workshop on Workload Characterization (WWC), Austin Texas, September 16, 2000.

Elizabeth S. Sorenson and J. Kelly Flanagan, Using Locality Surfaces to Characterize the SPECint 2000 Benchmark Suite, Third Annual IEEE Workshop on Workload Characterization (WWC), Austin Texas, September 16, 2000.

Jeff Penfold and J. Kelly Flanagan, A First Year Computer Organization Course on the Web: Make the Magic Disappear, IEEE Workshop on Computer Architecture Education (WCAE), Vancouver, BC, June 10, 2000.

F. Sorenson, E. Sorenson, K. Flanagan, H. Zhou, A System-Assisted Disk I/O Simulation Technique, IEEE International Workshop on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS '99), College Park, Maryland, October 24–28, 1999.

S. Peng, K. Flanagan, and F. Sorenson, Client-Based Web Prefetch Management, The Eighth International World Wide Web Conference, Toronto, Canada, May 11–14, 1999.

K. Flanagan and F. Sorenson, A National Trace Collection and Distribution Resource, 1999 SPEC Workshop, San Jose, California, January 25, 1999.

G. Judd, M. Clement, J. Peterson, B. Morse, and K. Flanagan, Performance Surface Prediction for WAN-Based Clusters, 31st Hawaii International Conference on System Sciences, Hawaii, January 6–9, 1998.

N. Thornock, X. Tu, and K. Flanagan, A Stochastic Disk I/O Simulation Technique, 1997 Winter Simulation Conference, Atlanta, December 7–10, 1997.

M. Clement, B. Morse, K. Flanagan, W. Wei and P. Crandall, The Chordal Spoke ATM Interconnection Network, Proceedings of the 1997 International Conference on Parallel and Distributed Techniques and Applications, Las Vegas, Nevada, June 1997.

M. Clement, K. Flanagan, and M. Steed, Cost Optimal Analysis for Workstation Clusters, Proceedings of the 1996 International Conference on Parallel and Distributed Processing Techniques and Applications, December 1996.

K. Flanagan, B. Nelson, J. Archibald, and G. Thompson, The Inaccuracy of Trace-Driven Simulation Using Incomplete Multiprogramming Trace Data, IEEE International Workshop on Modeling, Analysis and Simulation of Computer and Telecommunication Systems, February 1996.

G. Thompson, B. Nelson, and K. Flanagan, Transaction Processing Workloads — A Comparison to the SPEC Benchmarks Using Memory Hierarchy Performance Studies, IEEE International Workshop on Modeling, Analysis and Simulation of Computer and Telecommunication Systems, February 1996.

W. Wei, M. Clement, and K. Flanagan, The Round Table ATM Interconnection Network, Proceedings of the 1995 International Conference on Parallel and Distributed Processing Techniques and Applications, November 1995.

K. Flanagan, B. Nelson, J. Archibald, and K. Grimsrud, Incomplete Trace Data and Trace Driven Simulation, IEEE International Workshop on Modeling, Analysis and Simulation of Computer and Telecommunication Systems, January 1993.

K. Grimsrud, J. Archibald, B. Nelson, and K. Flanagan, BACH: A Hardware Measurement Tool for Microprocessor Systems, Invited paper for IEEE Asilomar Conference, October 1992.

K. Flanagan, B. Nelson, J. Archibald, and K. Grimsrud, BACH: BYU Address Collection Hardware, The Collection of Complete Traces, In Proceedings of the 6th International Conference on Modeling Techniques and Tools for Computer Performance Evaluation, September 1992.

B. Nelson, J. Archibald, and K. Flanagan, Performance Analysis of Inclusion Effects in Multi-level Multiprocessor Caches, IEEE Symposium on Parallel and Distributed Processing, December 1991.

K. Grimsrud and K. Flanagan, PARACHUTE: An Implementation of the Chordal Ring Architecture, Norddata 91, Norway, June 1991.

K. Flanagan, D. Morrell, R. Frost, C. Read, and B. Nelson, Vector Quantization Codebook Generation Using Simulated Annealing, IEEE International Conference on Acoustics, Speech, and Signal Processing, May 1989.

C. Read, D. Chabries, R. Christansen, and K. Flanagan, A Method for Computing the DFT of Vector Quantized Data, IEEE International Conference on Acoustics, Speech, and Signal Processing, May 1989.

K. Flanagan and B. Nelson, Microprocessor Design Using Path Programmable Logic, IEEE International Conference on Computer Design / VLSI in Computers, October 1988.

T. Li, B. Nelson, K. Flanagan, and C. Read, A Multiprogrammed Parallel Architecture FIR Digital Signal Processing, IEEE International Conference on Acoustics, Speech, and Signal Processing, April 1987.

OTHER PUBLICATIONS

Niki C. Thornock and J. Kelly Flanagan, A National Trace Collection and Distribution Resource, ACM SIGARCH Computer Architecture News, June 2001, Volume 29, Issue 3.

Elizabeth S. Sorenson and J. Kelly Flanagan, Using locality surfaces to characterize the SPECint 2000 benchmark suite, Workload Characterization for Emerging Computer Applications, pages 101–120, Kluwer Academic Publishers, 2001.

C. Rose and K. Flanagan, Complete Instruction Traces from Incomplete Address Traces (CITCAT), Poster Presentation, 1997 Winter Simulation Conference, Atlanta, December 7–10, 1997.

C. Rose and K. Flanagan, Complete Instruction Traces from Incomplete Address Traces (CITCAT), Computer Architecture News, December 1996.

PRESENTATIONS

Keynote, UVU AI Summit, March 29, 2023
UVU Summer University, March 2022
UVU UVSELF, January 2022
Keynote, UVU Data Summit, September 2021
University API Workshop, 2016
Indie Educational Technology Workshop, 2016
Office Professionals Association Conference, 2016
Internet Identity Workshop, 2015

Office Professionals Association Conference, 2012
Brigham Young University-Idaho Forum, 2010
InfoWorld Virtualization Executive Forum, 2007
InfoWorld Virtualization Executive Forum, 2006
Keynote, BYU Accessibility Banquet, 2006
Office Professionals Association Conference, 2005
BYU Devotional Address, 2002
Numerous BYU presentations, 2002–Present
Numerous presentations at Hewlett-Packard, Intel, Texas Instruments and Tandem, 1995–2000

THESES AND DISSERTATIONS SUPERVISED

Steven C. Cook, Dynamic Near Field Communication Pairing, 2013, Thesis
Elizabeth S. Sorenson, Cache Characterization and Performance Studies Using Locality Surfaces, 2005, Dissertation
Christopher R. Slade, On-Disk Sequence Cache (ODSC): Using Excess Disk Capacity to Increase Performance, 2005, Thesis
Myles G. Watson, Does the Halting Necessary for Hardware Trace Collection Inordinately Perturb the Results?, 2004, Thesis
Hyrum Carroll, A Trace-Driven Simulator for Palm OS Devices, 2004, Thesis
Franklin E. Sorenson, PODS: Physical Object Devices, 2004, Thesis
Vernon H. Mauery, Inheritance Models in Object-Oriented Hardware Using Physical Object Devices, 2004, Thesis
Darren Hart, Using Hardware Objects in Object Oriented Software Design, 2004, Thesis
Briton Barker, Cache Memory Analysis: Effects of the Kernel and the Justification of Associativity, 2001, Thesis
Elizabeth S. Sorenson, Locality Surfaces, 2001, Thesis
Alen Peacock, Dynamic Detection of Deterministic Disk Access Patterns, 2001, Thesis
Dong Lin, Reducing Energy Consumption using Disk Data Reorganization, 2000, Thesis
Niki Thornock, Using Set Sampling for Level Three Cache Studies, 1999, Thesis
Charlton Rose, CITCAT: Complete Instruction Traces from Cache Filtered Address Traces, 1999, Thesis
Song Peng, Client-Based Web Prefetch Management, 1998, Thesis
YiQiang Huang, Reducing WWW Latency Using Server-Based Prefetching Techniques, 1998, Thesis
Heng Zhou, A System-Assisted Disk I/O Simulation Technique, 1998, Thesis
Nianlong Yin, Reducing Application Load Time by Rearranging Disk Data, 1998, Thesis
Chulkee Sung, A Markov Model for Novell Netware Network Traffic, 1997, Thesis
Xiao-hong Tu, Disk Rearrangement on Novell Netware Systems, 1997, Thesis
Jun Su, Cache Optimization for Energy Efficient Memory Hierarchies, 1996, Thesis